IN THE CLAIMS:

We claim:

1. A timing system for controlling timing of data transfers within an embedded semiconductor memory system, the timing system comprising:

means for generating a bias signal, wherein the bias signal is biased in accordance with a data address of the memory system of data being transferred; and

means for receiving the bias signal and generating an output clock signal, wherein the timing of the output clock signal is programmable in accordance with the bias signal.

2. The timing system according to Claim 1, wherein the semiconductor memory is an embedded DRAM (eDRAM) memory.

3. The timing system according to Claim 1, wherein the bias signal is biased in accordance with the location of a memory cell corresponding to the memory address relative to a control region of the memory system.

4. The timing system according to Claim 1, wherein at least one of data, data address and control signal are held in a means for holding data, addresses and control signals, wherein an amount of time the at least one of data, data address and control signals are held is controlled by the output clock signal.

5. The timing system according to Claim 1, wherein the sum of an amount of time that the data is held in the means for holding and an amount of time that the data travels between a memory cell corresponding to the data address and the means for holding is a predetermined amount of time.

6. The timing system according to Claim 1, wherein a delay of the timing of the output clock signal is inversely proportional to a distance between a memory cell corresponding to the data address and the means for holding.

7. The timing system according to Claim 4, wherein during a first memory system clock cycle the amount of time is calculated and the at least one of data, data address and control signal are held in the means for holding, and during a subsequent second memory system clock cycle the at least one of data, data address and control signal are released from the means for holding in accordance with the amount of time and a different amount of time is calculated and a different at least one of data, data address and control signal are held in the means for holding for a subsequent data transfer.

8. The timing system according to Claim 3, wherein the data address includes first and second portions indicating the location of the memory cell relative to the control region in first and second dimensions, respectively.

9. The timing system according to Claim 1, wherein the means for generating the bias signal further includes a decoder circuit for decoding the data address and outputting at least one signal indicative of the data address.

10. The timing system according to Claim 9, wherein:

the means for generating the bias signal includes at least one bias stage for receiving a respective signal of the at least one signal indicative of the data address and outputting a signal biased relative to the received signal; and

the signal output by each bias stage of the at least one bias stage are combined to generate the bias signal.

11. The timing system according to Claim 8, wherein:

the means for generating the bias signal includes first and second biasing circuits;

the first and second portions of the incoming data transfer address are provided to the first and second biasing circuits, respectively, for generating first and second dimension bias signals; and

the means for generating the bias signal combines the first and second dimension bias signals to generate the bias signal.

12. The timing system according to Claim 1, wherein the means for generating the output clock signal receives a pulsating clock signal and includes first and second delay stages; and wherein:

the means for generating the output clock signal;

the pulsating clock signal and bias signal are provided to the first delay stage for generating an intermediate clock signal having a pulse rhythm similar to the pulsating clock signal and delayed by a first delay of the timing delay; and

the intermediate clock signal and the bias signal are provided to the second delay stage for generating the output clock signal having a pulse rhythm similar to the pulsating clock signal and delayed by a second delay of the timing delay.

13. The timing system according to Claim 12, wherein:

the first delay stage inverts the pulsating clock signal;

the first delay is the delay between the rising edge of a pulse of the pulsating clock signal and a falling edge of the inverted intermediate clock signal;

the second delay stage inverts the intermediate clock signal; and

the second delay is the delay between the rising edge of the intermediate clock signal and the falling edge of the output clock signal.

14. The timing system according to Claim 12, wherein the duration of the first and second delays is approximately the same.

15. The timing system according to Claim 1, wherein:

the means for generating the output clock signal receives a pulsating clock signal; and

the width of the pulses of the pulsating clock signal and the output clock signal are approximately the same.

16. The timing system according to Claim 12, wherein the bias signal is a bias current signal;

each of the first and second delay stages are delay controlled inverters having first and second nMOS devices and a pMOS device in series;

the pulsating clock signal is provided to gates of the first nMOS and pMOS devices of the first stage;

the bias signal is provided to gates of the second nMOS device of the first and second stages; and

the intermediate clock signal output from a node between the second nMOS and pMOS devices of the first delay stage is provided to the gates of the first nMOS and pMOS device of the second delay stage.

17. A biasing circuit for a timing system of an embedded semiconductor memory system, the biasing circuit comprising:

means for receiving a data address of a memory cell of the memory system;

means for processing the incoming address and outputting at least one signal indicative of the data address; and

means for generating a bias signal in accordance with the at least one signal indicative of the data address.

18. The biasing circuit according to Claim 17, wherein the at least one signal

indicative of the data address is indicative of the location of the memory cell, and the bias of the bias signal is generated in accordance with the location of the memory cell relative to a control region of the memory system.

19. The biasing circuit according to Claim 17, wherein data being transferred to or from the memory cell is held in a control region of the memory system, and the data is controllably released from the control region in accordance with the bias signal.

20. The biasing circuit according to Claim 19, wherein the sum of an amount of time that the data is held in the control region and an amount of time that the data travels between the memory cell and the control region is a predetermined amount of time.

21. A method for controlling timing a data transfers within an embedded semiconductor memory system comprising the steps of:

receiving a data address of a memory cell of the memory system transferring data;

processing the data address;

generating a bias signal in accordance with the processed data address;

generating a clock output signal having a delay in accordance with the bias signal; and

controlling release of data held in a control region of the memory system during a data transfer via the clock output signal.

22. The method according to Claim 21, wherein the data address is indicative of the location of the memory cell relative to the control region, and the bias signal is generated in accordance with the location of the memory cell corresponding to the processed data address.

23. The method according to Claim 22, wherein the sum of an amount of time that the data is held in the control region and an amount of time that the data travels between the memory cell and the control region is a predetermined amount of time.

24. The method according to Claim 21, wherein the delay of the clock output signal is relative to a system clock signal of the eDRAM system.